Pragmatic Verification Reuse in a Vertical World

Mark Litterick, Verilab, Germany

Consistent effective verification reuse is not being achieved!

- No closure on VR from external interfaces alone
- Real-world not conform to bottom-up reuse paradigm
- Validation of perfect chip is not enough
- Reuse is not for free

Active/Passive Misuse
- Low-level VCs are OK but environment ignores active/passive
to scorecard
- Drivers doing functional timeout checks
- Coverage defined in active components
- Configuration updates from sequence or driver
- Important messages from drivers
- Error injection traffic reported as a warning
- Passive components controlling end of test schedule

Problems of Scale
- Verification environment pulled together only in base-test
- Expect top-level to configure environment again
- Provide multiple interfaces to top-level
- Macro definitions having global scope
- Enumeration literals and types without package prefix

Additional Concerns
- Formal verification carried out at block-level
- Power-aware simulations introduced at top-level
- Inefficient design assertions generate performance bottleneck
- CDC operation not fully explored at block-level
- CDC waivers that prove to be invalid at top-level
- Uncontrollable or inappropriate AMS assertion performance

Active/Passive Guidelines
- Complete environment must consider active/passive
do not connect to active components
- Perform functional checks in passive components
- Collect functional coverage in passive components
- Update configuration only from passive components
- Generate important messages in passive components
- Promote warnings to errors in passive mode
- Do not control end of test from components in passive mode

Scale Guidelines
- Encapsulate all sub-components in an environment
- Encapsulate configuration objects
- Combine multiple interfaces into hierarchical interface
- Encapsulate SVA/HDL checks inside interface
- Avoid namespace collisions by using prefix per scope

Additional Guidelines
- Validate assumptions from formal in top-level
- Verification components need to be power-aware
- Enable only appropriate RTL assertions for top-level
- Reuse CDC assertions at top-level
- Exercise caution with bottom-up CDC waiver reuse
- Enable only appropriate AMS assertions for top-level

Tape-out Top Chip + Vertical Reuse = LESS + LESS + MORE $