VERIFICATION WORKSHOPS

Training & Consultancy Packages

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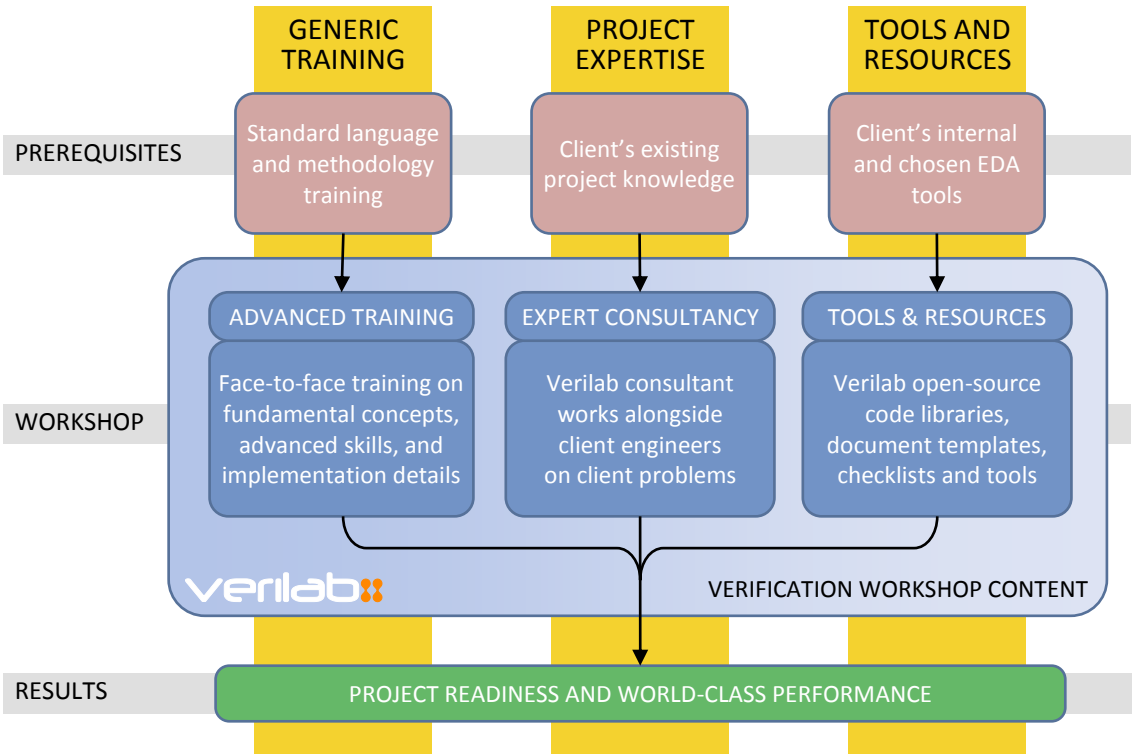
1. Introduction

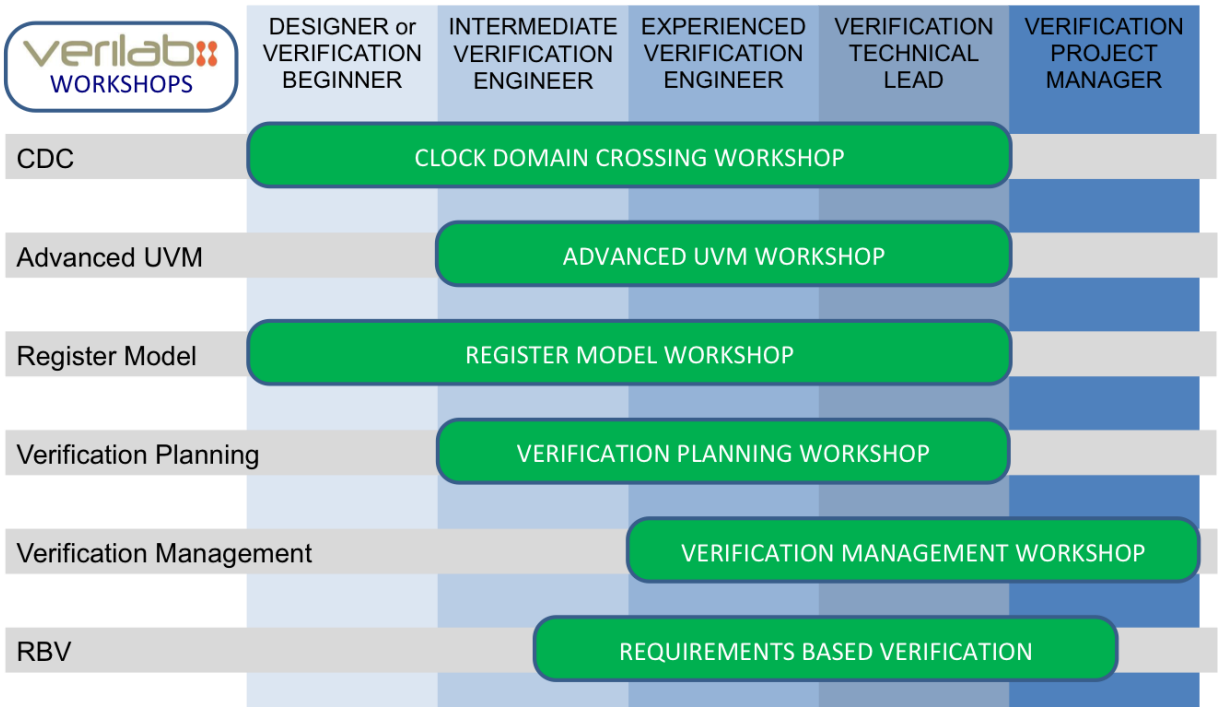
The Verilab ***Verification Workshops*** are a set of comprehensive *training* and *consultancy* packages targeting a wide range of subjects comprising the most important aspects of modern verification environment development, from verification planning and management through to advanced implementation strategies for key problems in this domain. The workshops can all be taken individually, or in combinations, and will not only increase the awareness and expertise of your verification teams, but will take them to the next level of mastery in this complex and challenging field.

Verilab's extensive practical experience in applying modern constrained-random coverage-driven verification techniques across a wide range of projects for many different clients has shown that there is a need for **advanced training** in verification techniques, methodologies and language-specific implementation details. However, this is not enough; the real power of the workshops is that the face-to-face interactive training sessions are coupled with **expert level consultancy** which allows the theory to be tightly bound to the clients applications, code-base, tool-flow and project-specific problems. Where appropriate, the workshops also provide **background resources** in the form of code libraries, templates, checklists, documents and tools in order to jump-start the effectiveness of the client teams. This combination, shown below, has proven to be an extremely effective way of transforming verification teams into world-class performers:



2. Workshop Portfolio

The current portfolio of Verilab *Verification Workshops* is shown in the following diagram, together with the target audience based on verification skill levels.



3. Workshop Descriptions

The following list provides a very brief overview of the currently available Verilab *Verification Workshops*. Each workshop also has a detailed syllabus document which is available from Verilab on request.

- **Clock Domain Crossing Workshop**:

  Targets the verification and design of Clock Domain Crossing (CDC) logic. Covers everything from fundamental problems with meta-stability and uncertainty, through synchronizer operation and assertion-based verification of CDC signals and jitter, concluding with back-end requirements such as STA and DFT. Increases awareness and expertise of CDC issues within the team, demonstrates effective assertion-based verification using SystemVerilog Assertions (SVA), improving design quality and verification effectiveness as a result. Suitable for design and verification engineers or managers working with applications that require multiple clock domains or asynchronous operation.

- **Advanced UVM Workshop**:

  Targets the detailed understanding and advanced application of SystemVerilog Universal Verification Methodology (UVM). Covers both generic language-independent verification concepts and their implementation in the UVM. Improves the effectiveness and expertise of all aspects of UVM within the verification team leading to faster verification environment development and improved quality. Suitable for any verification engineers with a working knowledge of SystemVerilog, an awareness of OVM or UVM, and exposure to constrained-random coverage-driven verification concepts in any implementation language or methodology (e.g. *e*, Vera, AVM, VMM, OVM or UVM).

- **Register Model Workshop**:

  Targets the detailed understanding of register modelling concepts, automatic generation of RTL and verification code for the model structure, and advanced modelling implementation in either *e* or UVM. As well as improving the effectiveness of register model generation, this workshop provides expert level material on solving difficult modelling problems such as timing accuracy, managing uncertainty, and passive modelling of side-effects and field interactions. Suitable for intermediate to advanced verification engineers with a working knowledge of e or OVM/UVM, design engineers involved in the register generation flow, as well as the generation tool provider or integrators.

- **Verification Planning Workshop**:

  Targets the detailed planning of modern verification environments from an *implementation engineer* perspective; includes such aspects as requirements capture, verification plan generation, task analysis, effort estimation, and achieving closure. The primary outputs from this workshop are effective verification plan documentation generation and associated processes, as well as improved skills in all aspects of planning, execution, reporting and delivery. Suitable for all verification engineers and technical managers involved in actual verification tasks.

- **Verification Management Workshop**:

  Targets all aspects of verification management in modern complex environments from an *engineering management* perspective; includes such aspects as requirements capture and tracking, verification planning and progress measurement, task analysis and effort estimation, risk analysis, project metrics and achieving closure. The goal of this workshop is to increase awareness of all these sometimes-competing requirements in order to put them into context, enabling better control over the process,

more appropriate risk management, and therefore enabling project milestones to be achieved on time. Suitable for lead engineers and technical managers with verification project responsibilities.

- **Requirements Based Verification Workshop**:

  RBV is a structured approach to planning and organizing verification projects which aims for efficiency by allowing stakeholders visibility into the size, scope, progress and risk of the overall verification process. By providing risk-based visibility at all stages in the development this approach helps ensure that verification proceeds with few surprises. Extremely detailed requirements capture and analysis guidance, combined with risk-based prioritization also means that this workshop is also relevant for teams using any standard plan-based verification flow. Suitable for all verification engineers and technical managers with verification planning and management responsibilities.

The workshop offerings are constantly evolving and several more topics are currently under development. If you like the concept, but would like to see another topics in the portfolio, then please contact Verilab to discuss.

4. Prerequisites & Generic Training

It is assumed that workshop attendees will have a working knowledge of modern constrained-random coverage-driven verification concepts and some exposure to SystemVerilog and either OVM or UVM (or *e* where appropriate). Verilab and its training partners can also provide customized training on the following related topics:

- **SystemVerilog:** basic, intermediate and advanced training - assertion-based verification using SVA
- **UVM:** getting started with UVM - OVM to UVM migration - SystemVerilog/UVM for Specman/e users
- ***e*:** Specman/e for SystemVerilog/UVM users

5. Duration

A typical workshop lasts three to five days, although this can be varied depending on your existing level of experience and the actual consultancy content. This includes approximately two to three full days of taught presentations, distributed among the consulting sessions where the theory from the presentations is applied to real problems from your domain and code base.

6. About Verilab

Verilab is an elite international team of verification experts. We specialize in solving the toughest problems in VLSI functional verification, from chip rescue and critical path pruning, through sophisticated verification IP development, to complete methodology re-engineering. Our consultants are skilled across the full range of the most powerful modern tools, technologies and methods. And as well as deploying those in new scenarios, we are experienced in making best practices fit into existing flows.

Established in 2000, we now serve clients across Europe and North America from our sites in Texas, Oregon, Canada, Germany and Britain. We can deploy the best consultants available to your project. Let us help you find, corner and kill those bugs.

Refer to www.verilab.com for more details.

7. Contact

For further information or detailed syllabus on any of the Verilab *Verification Workshops,* please contact us via email: info@verilab.com.